**Cell Description:**This is a standard full adder (FA) cell. This cell has 3 inputs A, B, and Cin, along with two outputs Sum and Cout. The function of this cell adds the two operands (A, and B) together along with the Cin which is the carry-in value from the previous stage of the adder. Once added together, the cell produces a Sum value, and a Cout (carry out) value if necessary.

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cin** | **A** | **B** | **Sum** |  |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Behavioral Verilog:**

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| FAX1 | 27.0 | 40.8 |
| FAX2 | 27.0 | 40.8 |

**Performance:**

**Propagation Delay (Rising Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| FAX1 | 0.545184 | 4.956384 |
| FAX2 | 0.547069 | 4.692737 |

**Output Rise Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| FAX1 | 0.236312 | 3.636292 |
| FAX2 | 0.217119 | 5.140482 |

**Propagation Delay (Falling Outputs):**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| FAX1 | 0.661016 | 6.331661 |
| FAX2 | 0.590398 | 5.12905 |

**Output Fall Time:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Min. (nS)** | **Max. (nS)** |
| FAX1 | 0.293497 | 4.717055 |
| FAX2 | 0.231074 | 3.558365 |

**Logic Symbol:**The following figure displays the symbol for the full adder. The symbol is the same for both available drive strengths.

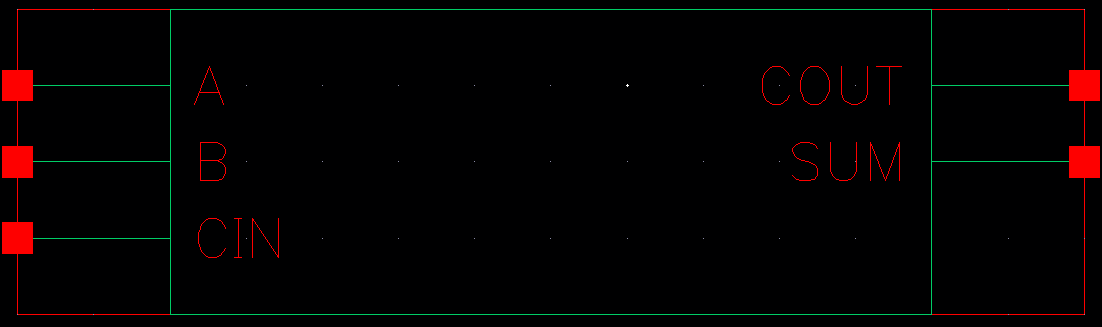
****

Figure 1: Symbol View for the FA cell.

**CMOS Schematic:**

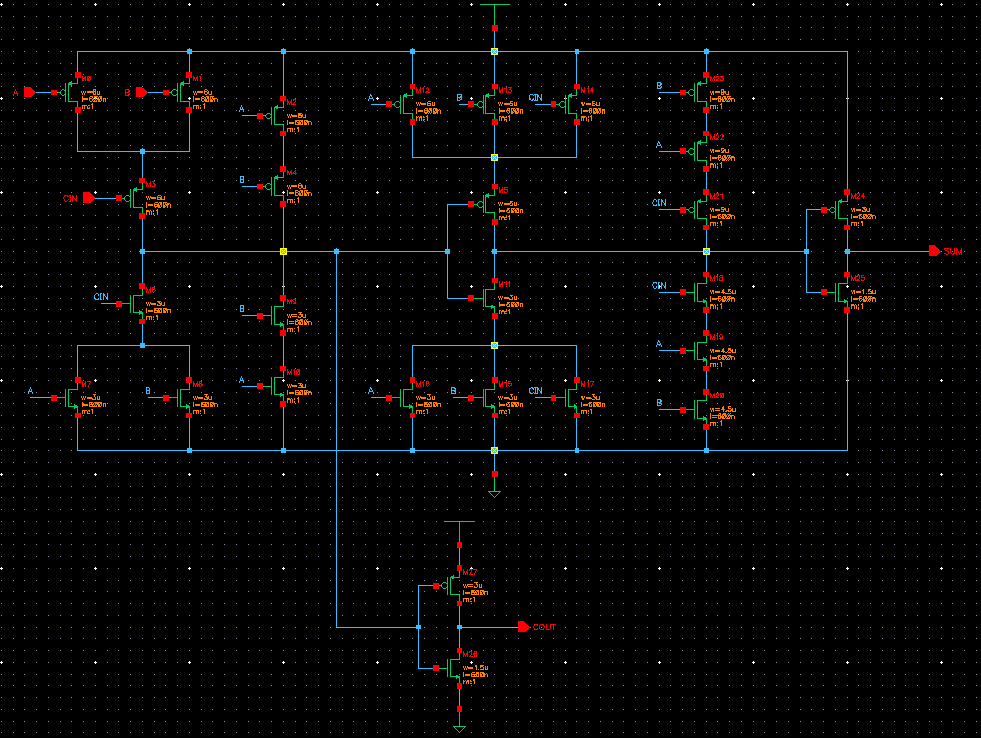
****

Figure 2: CMOS schematic view for the FAX1 cell.

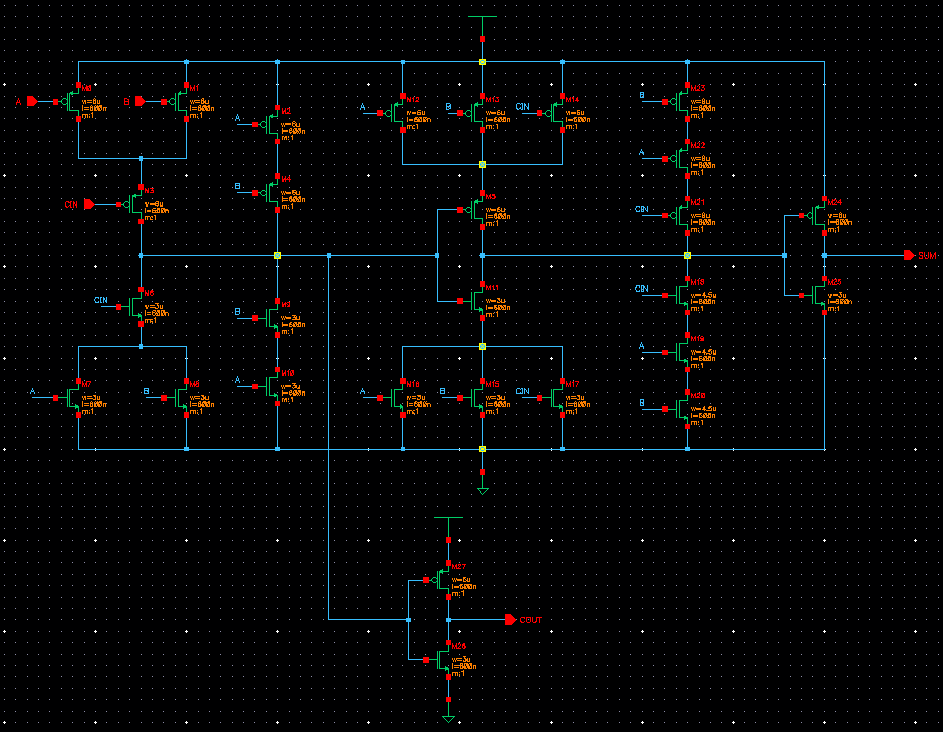
****

Figure 3: CMOS schematic view for the FAX2 cell.

**CMOS Layout:**

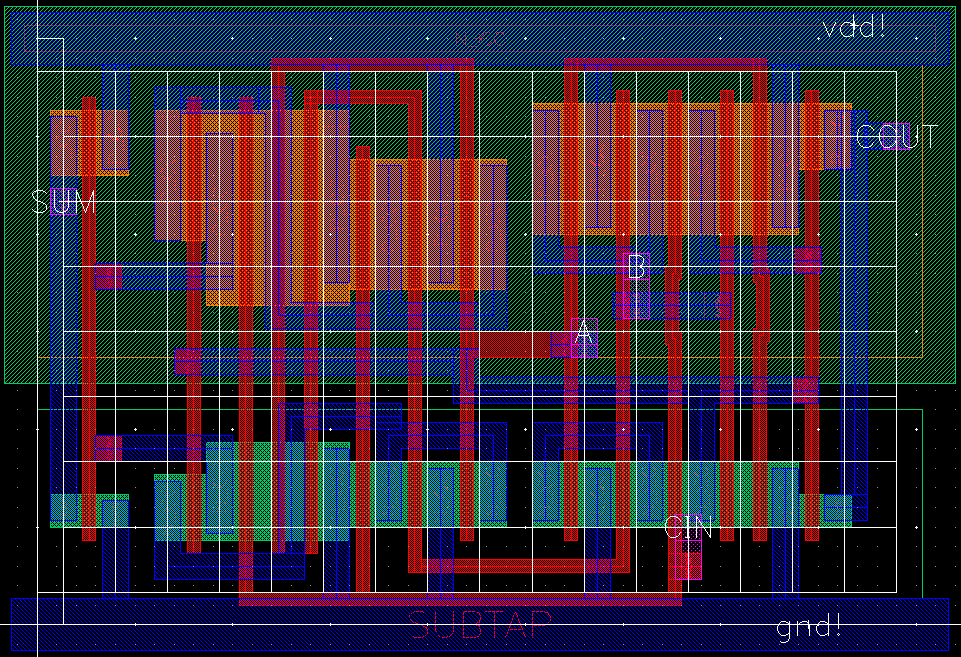
****

Figure 4: CMOS layout view for the FAX1 cell.

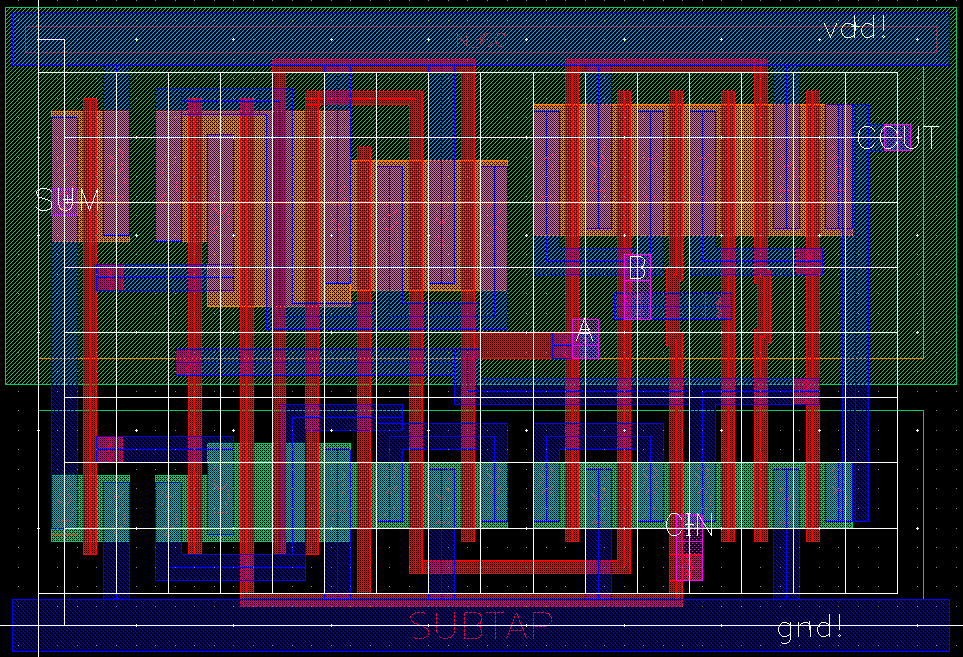
****

Figure 5: CMOS layout view for the FAX2 cell.